Національний технічний університет України

«Київський політехнічний інститут»

Факультет інформатики та обчислювальної техніки

Кафедра обчислювальної техніки

**Лабораторна робота №8**

*з предмету: «ТПКС»*

*по темі:*

«Моделювання логічних схем у середовищі Active-HDL»

Виконав: студент ФІОТ

групи ІО-92

Петрук В.О.

Київ 2012р.

**Мета:** Здобуття навичок з функціонального моделювання логічних схем у

середовищі Active-HDL.

**Завдання**

1. Створити нове робоче середовище (Workspace) в Active-HDL.

2. Створити VHDL-проект.

3. Завантажити VHDL-спеціфікацію з попередньої роботи (Лаб.7)

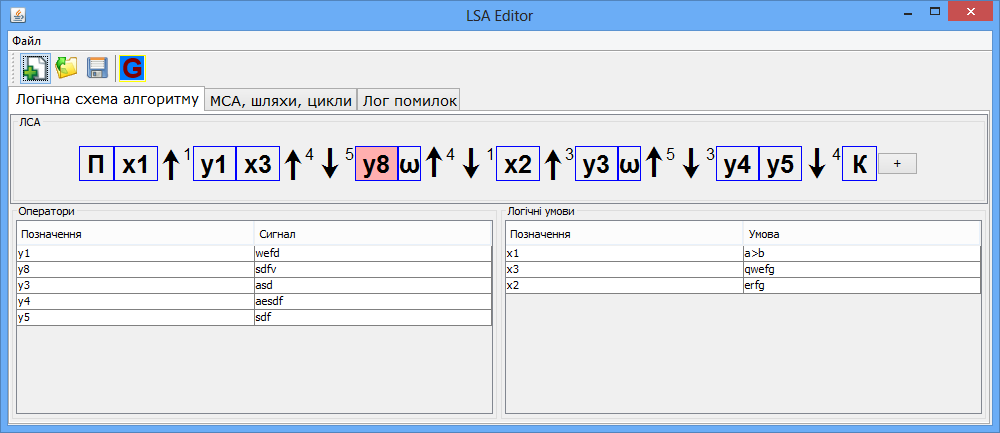
4. Перевірити коректність функцій переходів і збудження тригерів у редакторі Waveform Editor.

5. Результати занотувати в протокол.

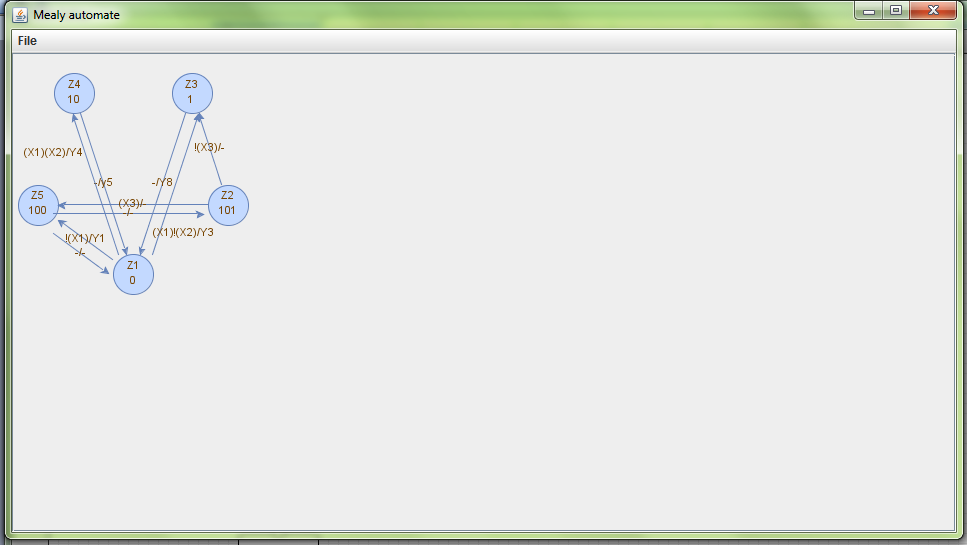
Для побудови на заданому базисі використовувалися результати мінімізації (ДКНФ). Обрана форма І-НЕ / І.

**Перевірка роботи**

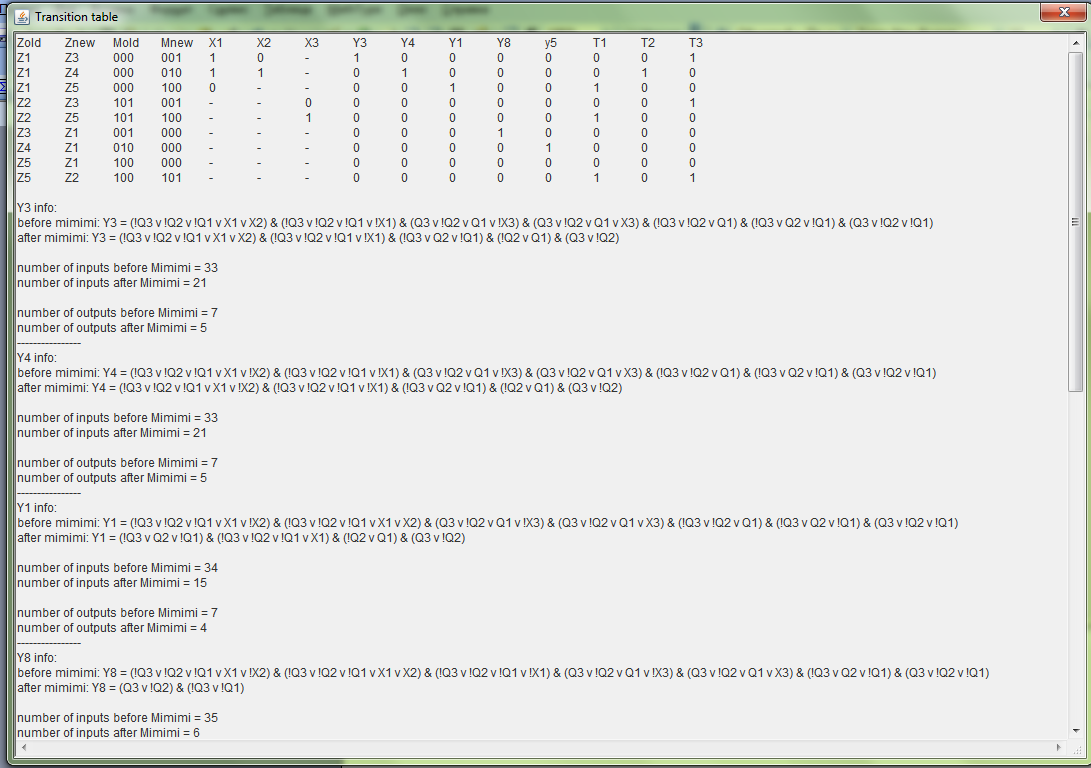
Вихідний алгоритм:



**Синтезований автомат:**



**Структурна таблиця:**



**Дані для перевірки роботи:**

Zold Znew Mold Mnew X1 X2 X3 Y3 Y4 Y1 Y8 y5 T1 T2 T3

Z1 Z3 000 001 1 0 - 1 0 0 0 0 0 0 1

Z1 Z4 000 010 1 1 - 0 1 0 0 0 0 1 0

Z1 Z5 000 100 0 - - 0 0 1 0 0 1 0 0

Z2 Z3 101 001 - - 0 0 0 0 0 0 0 0 1

Z2 Z5 101 100 - - 1 0 0 0 0 0 1 0 0

Z3 Z1 001 000 - - - 0 0 0 1 0 0 0 0

Z4 Z1 010 000 - - - 0 0 0 0 1 0 0 0

Z5 Z1 100 000 - - - 0 0 0 0 0 0 0 0

Z5 Z2 100 101 - - - 0 0 0 0 0 1 0 1

Y3 = (!Q3 v !Q2 v !Q1 v X1 v X2) & (!Q3 v !Q2 v !Q1 v !X1) & (!Q3 v Q2 v !Q1) & (!Q2 v Q1) & (Q3 v !Q2)

Y4 = (!Q3 v !Q2 v !Q1 v X1 v !X2) & (!Q3 v !Q2 v !Q1 v !X1) & (!Q3 v Q2 v !Q1) & (!Q2 v Q1) & (Q3 v !Q2)

Y1 = (!Q3 v Q2 v !Q1) & (!Q3 v !Q2 v !Q1 v X1) & (!Q2 v Q1) & (Q3 v !Q2)

Y8 = (Q3 v !Q2) & (!Q3 v !Q1)

y5 = (!Q3 v !Q2 v !Q1) & (!Q2 v Q1) & (Q3 v !Q2)

T1 = (Q3 v !Q2 v Q1 v !X3) & (!Q3 v !Q2 v Q1) & (!Q3 v Q2 v !Q1) & (Q3 v !Q2 v !Q1) & (!Q3 v !Q2 v !Q1 v X1)

T2 = (!Q3 v !Q2 v !Q1 v X1 v !X2) & (!Q3 v !Q2 v !Q1 v !X1) & (!Q3 v Q2 v !Q1) & (!Q2 v Q1) & (Q3 v !Q2)

T3 = (!Q3 v !Q2 v !Q1 v X1 v X2) & (!Q3 v !Q2 v !Q1 v !X1) & (Q3 v !Q2 v Q1 v X3) & (!Q3 v !Q2 v Q1) & (!Q3 v Q2 v !Q1) & (Q3 v !Q2 v !Q1)

**Вміст VHDL-файла:**

entity MyEntity is

port (

X1 : in bit;

X2 : in bit;

X3 : in bit;

Y3 : out bit;

Y4 : out bit;

Y1 : out bit;

Y8 : out bit;

y5 : out bit;

T1 : out bit;

Q1 : in bit;

T2 : out bit;

Q2 : in bit;

T3 : out bit;

Q3 : in bit

);

end entity MyEntity;

architecture MyArchitecture of MyEntity is

signal temp\_0,temp\_1,temp\_2,temp\_3,temp\_5,temp\_6,temp\_7,temp\_8,temp\_9,temp\_10,temp\_12,temp\_13,temp\_14,temp\_15,temp\_17,temp\_18,temp\_19,temp\_20,temp\_21,temp\_22,temp\_24,temp\_25,temp\_27,temp\_28,temp\_29,temp\_30,temp\_33,temp\_34,temp\_36,temp\_37,temp\_38,temp\_40,temp\_42,temp\_43,temp\_44,temp\_45,temp\_46,temp\_48,temp\_49,temp\_50,temp\_52,temp\_53,temp\_54,temp\_55,temp\_57,temp\_58,temp\_59,temp\_60,temp\_61,temp\_62,temp\_64,temp\_65,temp\_66,temp\_67,temp\_69,temp\_70,temp\_72,temp\_73,temp\_74,temp\_75,temp\_76,temp\_77 : bit;

begin

P\_0: process(Q3,Q2,Q1)

begin

temp\_0 <= (not Q3 and not Q2 and not Q1 );

end process P\_0;

P\_1: process(X1,X2)

begin

temp\_1 <= (X1 and X2 );

end process P\_1;

P\_2: process(temp\_0,temp\_1)

begin

temp\_2 <= not (temp\_0 and temp\_1 );

end process P\_2;

P\_3: process(Q3,Q2,Q1)

begin

temp\_3 <= (not Q3 and not Q2 and not Q1 );

end process P\_3;

P\_5: process(temp\_3,X1)

begin

temp\_5 <= not (temp\_3 and not X1 );

end process P\_5;

P\_6: process(Q3,Q2,Q1)

begin

temp\_6 <= not (not Q3 and Q2 and not Q1 );

end process P\_6;

P\_7: process(Q2,Q1)

begin

temp\_7 <= not (not Q2 and Q1 );

end process P\_7;

P\_8: process(Q3,Q2)

begin

temp\_8 <= not (Q3 and not Q2 );

end process P\_8;

P\_9: process(temp\_2,temp\_5,temp\_6)

begin

temp\_9 <= (temp\_2 and temp\_5 and temp\_6 );

end process P\_9;

P\_10: process(temp\_7,temp\_8)

begin

temp\_10 <= (temp\_7 and temp\_8 );

end process P\_10;

P\_11: process(temp\_9,temp\_10)

begin

Y3 <= (temp\_9 and temp\_10 );

end process P\_11;

P\_12: process(Q3,Q2,Q1)

begin

temp\_12 <= (not Q3 and not Q2 and not Q1 );

end process P\_12;

P\_13: process(X1,X2)

begin

temp\_13 <= (X1 and not X2 );

end process P\_13;

P\_14: process(temp\_12,temp\_13)

begin

temp\_14 <= not (temp\_12 and temp\_13 );

end process P\_14;

P\_15: process(Q3,Q2,Q1)

begin

temp\_15 <= (not Q3 and not Q2 and not Q1 );

end process P\_15;

P\_17: process(temp\_15,X1)

begin

temp\_17 <= not (temp\_15 and not X1 );

end process P\_17;

P\_18: process(Q3,Q2,Q1)

begin

temp\_18 <= not (not Q3 and Q2 and not Q1 );

end process P\_18;

P\_19: process(Q2,Q1)

begin

temp\_19 <= not (not Q2 and Q1 );

end process P\_19;

P\_20: process(Q3,Q2)

begin

temp\_20 <= not (Q3 and not Q2 );

end process P\_20;

P\_21: process(temp\_14,temp\_17,temp\_18)

begin

temp\_21 <= (temp\_14 and temp\_17 and temp\_18 );

end process P\_21;

P\_22: process(temp\_19,temp\_20)

begin

temp\_22 <= (temp\_19 and temp\_20 );

end process P\_22;

P\_23: process(temp\_21,temp\_22)

begin

Y4 <= (temp\_21 and temp\_22 );

end process P\_23;

P\_24: process(Q3,Q2,Q1)

begin

temp\_24 <= not (not Q3 and Q2 and not Q1 );

end process P\_24;

P\_25: process(Q3,Q2,Q1)

begin

temp\_25 <= (not Q3 and not Q2 and not Q1 );

end process P\_25;

P\_27: process(temp\_25,X1)

begin

temp\_27 <= not (temp\_25 and X1 );

end process P\_27;

P\_28: process(Q2,Q1)

begin

temp\_28 <= not (not Q2 and Q1 );

end process P\_28;

P\_29: process(Q3,Q2)

begin

temp\_29 <= not (Q3 and not Q2 );

end process P\_29;

P\_30: process(temp\_24,temp\_27,temp\_28)

begin

temp\_30 <= (temp\_24 and temp\_27 and temp\_28 );

end process P\_30;

P\_32: process(temp\_30,temp\_29)

begin

Y1 <= (temp\_30 and temp\_29 );

end process P\_32;

P\_33: process(Q3,Q2)

begin

temp\_33 <= not (Q3 and not Q2 );

end process P\_33;

P\_34: process(Q3,Q1)

begin

temp\_34 <= not (not Q3 and not Q1 );

end process P\_34;

P\_35: process(temp\_33,temp\_34)

begin

Y8 <= (temp\_33 and temp\_34 );

end process P\_35;

P\_36: process(Q3,Q2,Q1)

begin

temp\_36 <= not (not Q3 and not Q2 and not Q1 );

end process P\_36;

P\_37: process(Q2,Q1)

begin

temp\_37 <= not (not Q2 and Q1 );

end process P\_37;

P\_38: process(Q3,Q2)

begin

temp\_38 <= not (Q3 and not Q2 );

end process P\_38;

P\_39: process(temp\_36,temp\_37,temp\_38)

begin

y5 <= (temp\_36 and temp\_37 and temp\_38 );

end process P\_39;

P\_40: process(Q3,Q2,Q1)

begin

temp\_40 <= (Q3 and not Q2 and Q1 );

end process P\_40;

P\_42: process(temp\_40,X3)

begin

temp\_42 <= not (temp\_40 and not X3 );

end process P\_42;

P\_43: process(Q3,Q2,Q1)

begin

temp\_43 <= not (not Q3 and not Q2 and Q1 );

end process P\_43;

P\_44: process(Q3,Q2,Q1)

begin

temp\_44 <= not (not Q3 and Q2 and not Q1 );

end process P\_44;

P\_45: process(Q3,Q2,Q1)

begin

temp\_45 <= not (Q3 and not Q2 and not Q1 );

end process P\_45;

P\_46: process(Q3,Q2,Q1)

begin

temp\_46 <= (not Q3 and not Q2 and not Q1 );

end process P\_46;

P\_48: process(temp\_46,X1)

begin

temp\_48 <= not (temp\_46 and X1 );

end process P\_48;

P\_49: process(temp\_42,temp\_43,temp\_44)

begin

temp\_49 <= (temp\_42 and temp\_43 and temp\_44 );

end process P\_49;

P\_50: process(temp\_45,temp\_48)

begin

temp\_50 <= (temp\_45 and temp\_48 );

end process P\_50;

P\_51: process(temp\_49,temp\_50)

begin

T1 <= (temp\_49 and temp\_50 );

end process P\_51;

P\_52: process(Q3,Q2,Q1)

begin

temp\_52 <= (not Q3 and not Q2 and not Q1 );

end process P\_52;

P\_53: process(X1,X2)

begin

temp\_53 <= (X1 and not X2 );

end process P\_53;

P\_54: process(temp\_52,temp\_53)

begin

temp\_54 <= not (temp\_52 and temp\_53 );

end process P\_54;

P\_55: process(Q3,Q2,Q1)

begin

temp\_55 <= (not Q3 and not Q2 and not Q1 );

end process P\_55;

P\_57: process(temp\_55,X1)

begin

temp\_57 <= not (temp\_55 and not X1 );

end process P\_57;

P\_58: process(Q3,Q2,Q1)

begin

temp\_58 <= not (not Q3 and Q2 and not Q1 );

end process P\_58;

P\_59: process(Q2,Q1)

begin

temp\_59 <= not (not Q2 and Q1 );

end process P\_59;

P\_60: process(Q3,Q2)

begin

temp\_60 <= not (Q3 and not Q2 );

end process P\_60;

P\_61: process(temp\_54,temp\_57,temp\_58)

begin

temp\_61 <= (temp\_54 and temp\_57 and temp\_58 );

end process P\_61;

P\_62: process(temp\_59,temp\_60)

begin

temp\_62 <= (temp\_59 and temp\_60 );

end process P\_62;

P\_63: process(temp\_61,temp\_62)

begin

T2 <= (temp\_61 and temp\_62 );

end process P\_63;

P\_64: process(Q3,Q2,Q1)

begin

temp\_64 <= (not Q3 and not Q2 and not Q1 );

end process P\_64;

P\_65: process(X1,X2)

begin

temp\_65 <= (X1 and X2 );

end process P\_65;

P\_66: process(temp\_64,temp\_65)

begin

temp\_66 <= not (temp\_64 and temp\_65 );

end process P\_66;

P\_67: process(Q3,Q2,Q1)

begin

temp\_67 <= (not Q3 and not Q2 and not Q1 );

end process P\_67;

P\_69: process(temp\_67,X1)

begin

temp\_69 <= not (temp\_67 and not X1 );

end process P\_69;

P\_70: process(Q3,Q2,Q1)

begin

temp\_70 <= (Q3 and not Q2 and Q1 );

end process P\_70;

P\_72: process(temp\_70,X3)

begin

temp\_72 <= not (temp\_70 and X3 );

end process P\_72;

P\_73: process(Q3,Q2,Q1)

begin

temp\_73 <= not (not Q3 and not Q2 and Q1 );

end process P\_73;

P\_74: process(Q3,Q2,Q1)

begin

temp\_74 <= not (not Q3 and Q2 and not Q1 );

end process P\_74;

P\_75: process(Q3,Q2,Q1)

begin

temp\_75 <= not (Q3 and not Q2 and not Q1 );

end process P\_75;

P\_76: process(temp\_66,temp\_69,temp\_72)

begin

temp\_76 <= (temp\_66 and temp\_69 and temp\_72 );

end process P\_76;

P\_77: process(temp\_73,temp\_74,temp\_75)

begin

temp\_77 <= (temp\_73 and temp\_74 and temp\_75 );

end process P\_77;

P\_78: process(temp\_76,temp\_77)

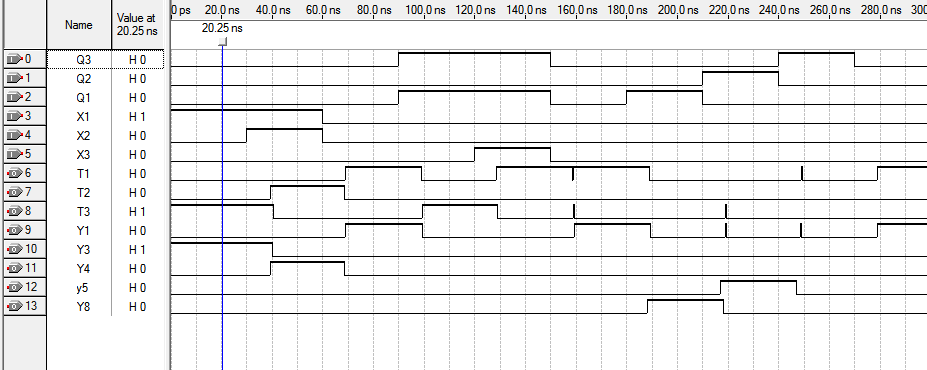
begin

T3 <= (temp\_76 and temp\_77 );

end process P\_78;

end architecture MyArchitecture;

**Результати симуляції (програма Quartus):**



**Висновок**

На основі раніше створеного VHDL-файла створено проект в програмному комплексі Quartus та проведено моделювання часових функцій. Результати симуляції повністю відповідають даним структурної таблиці, що означає, що синтез схеми виконаний правильно.